REMARKS

Claims 1-20 are pending. Applicant thanks the Examiner for the in-person interview held on November 25, 2003. By this amendment, claims 1 and 11 are amended. No new matter is introduced. Support for the amendments may be found at least on page 4, lines 12-16, page 5, lines 14-18, page 9, line 20, and page 10, line 9 of the specification. Reconsideration and allowance of all pending claims is respectfully requested in view of the preceding amendments and following remarks.

Claim Rejections Under 35 U.S.C. §102

Claims 1-6, 8, 10-16, 18, and 20 are rejected under 35 U.S.C. §102 (b) over U.S. Patent 6,317,763 to Vatinel (hereafter Vatinel). This rejection is respectfully traversed.

Vatinel is directed to circuits, barrel shifters, and methods for manipulating a bit pattern. However, Vatinel does not disclose or suggest "a plurality of dual rail Domino logic gates ... the control signals include a plurality of control lines to provide for multiple shifting operations ... wherein each of the logic gates receives one data input using the single data transistor and receives other data inputs from adjacent logic gates using the plurality of shared data lines to reduce the number of data transistors required" as recited in amended claim 1.

The logic circuit for use in a multiplexer as recited in claim 1 uses data sharing among transistors in order to reduces the number of transistors required by each dual rail Domino logic gate. Referring to page 4, lines 12-16 of the specification, "instead of using a separate transistor for each input data line to each logic gate, only a single transistor is required in this example for a particular data input. The other data inputs are received from adjacent or other logic gates using shared data lines." Vatinel does not disclose or suggest the feature of enabling all of the logic gates to share a single data transistor for each data input. Therefore, amended claim 1 is allowable.

Claims 2-6, 8, and 10 are allowable because they depend from allowable claim 1 and for the additional features they recite.

Regarding claim 11, for at least the same reason as noted above with respect to claim 1, Vatinel does not disclose or suggest "providing a plurality of dual rail Domino logic gates ... the control signals include a plurality of control lines to provide for multiple shifting operations ... wherein each of the logic gates receives one data input using the single data transistor and receives other data inputs from adjacent logic gates using the plurality of shared data lines to reduce the number of data transistors required" as recited in amended claim 11. Therefore, amended claim 11 is allowable.

Claims 12-16, 18, and 20 are allowable because they depend from allowable claim 11 and for the additional features they recite. Withdrawal of the rejection of claims 1-6, 8, 10-16, 18, and 20 under 35 U.S.C. §102 (b) is respectfully requested.

Claim Rejections Under 35 U.S.C. §103

Claims 7 and 17 are rejected under 35 U.S.C. §103 (a) over Vatinel in view of U.S. Patent 5,961,575 to Hervin et al. (hereafter Hervin). This rejection is respectfully traversed.

Claims 7 and 17 are allowable because they depend from allowable claims 1 and 11, respectively, and for the additional features they recite. Withdrawal of the rejection of claims 7 and 17 under 35 U.S.C. §103 (a) is respectfully requested.

Claims 9 and 19 are rejected under 35 U.S.C. §103 (a) over Vatinel. This rejection is respectfully traversed.

Claims 9 and 19 are allowable because they depend from allowable claims 1 and 11, respectively, and for the additional features they recite. Withdrawal of the rejection of claims 9 and 19 under 35 U.S.C. §103 (a) is respectfully requested.

In view of the above remarks, Applicant respectfully submits that the application is in condition for allowance. Prompt examination and allowance are respectfully requested.

Should the Examiner believe that anything further is desired in order to place the application in even better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

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